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Total Number of Pages: 02

Course: B.Tech/IDD  
Sub\_Code: RCS3C001

337-22/01/2025--48  
3rd Semester Back Examination: 2024-25  
SUBJECT: Digital Logic Design  
BRANCH(S): CSIT, CSEDS, CST, CSEAIML, CSEAI, CSE, CSE, IT  
Time: 3 Hours  
Max Marks: 100  
Q.Code: R563

Answer Question No.1 (Part-I) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Part-I

Q1 Answer the following questions: (2 x 10)

- Convert the decimal number 108.364 to binary equivalent.
- Show how to connect NAND gates to get an AND gate and OR gate.
- Find the equivalent Gray code for  $[10110]_2$ .
- Implement full adder using half adders.
- Compare the function of decoder and encoder.
- Prepare the truth table for JK Flip flop.
- Draw the circuit diagram of ring Counter.
- How many flip-flops are required to build a binary counter that counts from 0 to 7?
- Define Hazards. How it can be avoided?
- How can a race in digital circuits can be avoided?

Part-II

Q2 Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve) (6 x 8)

- Find the Minimized logic function using K-Maps.  $F(A, B, C, D) = \sum m(1, 3, 5, 8, 9, 11, 15) + d(2, 13)$ . Implement the minimal SOP using NAND and NOR gates.
- Describe about multiplexer and simplify the following function using 8x1 Mux  $F = \sum(0, 1, 3, 4, 8, 9, 15)$ .
- Explain the concept of priority encoder with truth table, Boolean expression and logic diagram.
- Discuss about the purpose of decoder and Implement a full adder and full subtractor using decoder.
- Using D flip-flop, design a synchronous counter which counts in the sequence 000, 001, 010, 011, 100, 101, 110, 111, 000.
- Summarize 4-bit SISO, SIPO, PIPO, and PISO shift register with block diagrams.
- Explain ASM chart for binary multiplier.
- Design a MOD-4 synchronous counter using only D flipflops.

- i) Design a MOD-11 asynchronous counter using only T flipflops.
- j) Draw and explain the operation of MOD-14 Ring counter using any flipflops.
- k) Describe how a state graph for a sequential machine can be converted to an equivalent ASM chart?
- l) Develop a state table, characteristic table and an excitation table for SR Flip Flop.

### Part-III

#### Only Long Answer Type Questions (Answer Any Two out of Four)

- Q3** Determine the minimal Sum of Products for the following function  $F(w, x, y, z) = \sum m(1, 3, 4, 5, 9, 10, 11) + \sum d(3, 4, 11)$  using Quine McCluskey method and apply DeMorgan's theorem for NAND - NOR implementation. **(16)**
- Q4** Design a certain logic circuit using 4 x 1 Multiplexer which has four inputs A, B, C, and D. The output X of the circuit is logic 1 if two or more inputs are logic 1. **(16)**
- Q5** Design an Asynchronous sequential circuit with input A and B and an output Y. Initially at any time if both the inputs are 0, the output, Y = 0. When A or B = 1, Y = 1. When the other input also become 1, Y = 0. The output stays at 0 until circuit goes back to initial state. **(16)**
- Q6** a) Examine a synchronous MOD-6 counter and explain the operation. **(8x2)**  
 b) Analyze the MOD-6 counter with an appropriate waveform.